Amendments to the Claims

This listing of the Claims will replace all prior versions and listings of the claims in this patent application.

Listing of the Claims

1-93. (canceled)

94. (currently amended) An electronic component ~~semiconductor chip or wafer~~ comprising:

a semiconductor substrate having multiple semiconductor devices;

an interconnecting metallization structure over said semiconductor substrate;

an insulating ~~passivation~~ layer over said interconnecting metallization structure; and

an upper metallization structure over said insulating ~~passivation~~ layer, wherein said upper metallization structure comprises a metal layer having a thickness of between 2 and 100 μm, and ~~and comprising gold,~~ wherein said upper metallization structure connects ~~comprises a connecting portion connecting~~ multiple portions of said interconnecting metallization structure.

95. (currently amended) The electronic component ~~semiconductor chip or wafer~~ of claim 94, wherein said insulating ~~passivation~~ layer comprises a topmost nitride layer of said semiconductor chip or wafer.

96. (currently amended) The electronic component ~~semiconductor chip or wafer~~ of claim 94, wherein said insulating ~~passivation~~ layer comprises a passivation layer. ~~a topmost oxide layer of said semiconductor chip or wafer.~~

97. (currently amended) The electronic component ~~semiconductor chip or wafer~~ of claim 94, wherein said insulating ~~passivation~~ layer comprises a topmost CVD-formed ~~insulation~~ layer~~,~~ ~~formed using a CVD process,~~ of said semiconductor chip or wafer.

98. (currently amended) The electronic component ~~semiconductor chip or wafer~~ of claim 94, wherein said interconnecting metallization structure comprises a first contact pad exposed by an opening in said insulating ~~passivation~~ layer, and said upper metallization structure comprises a second contact pad connected to said first contact pad, wherein the positions of said first and second contact pads from a top view are different.

99. (currently amended) The electronic component ~~semiconductor chip or wafer~~ of claim 94, wherein said metal layer comprises gold. ~~gold comprises a gold layer having a thickness of between 2 and 100 μm.~~

100. (currently amended) The electronic component ~~semiconductor chip or wafer~~ of claim 99, wherein said upper metallization structure further comprises an underlying ~~a~~ metal layer under said metal ~~gold~~ layer, wherein said underlying metal layer comprises titanium tungsten.

101. (previously added) The electronic component ~~semiconductor chip or wafer~~ of claim 94, wherein said semiconductor substrate comprises silicon.

102. (currently amended) The electronic component ~~semiconductor chip or wafer~~ of claim 94 further comprising a topmost polymer layer over said insulating ~~passivation~~ layer, wherein said upper metallization structure ~~comprises an upper metal layer~~ is over said topmost polymer layer.

103. (currently amended) The electronic component ~~semiconductor chip or wafer~~ of claim 94, wherein said interconnecting metallization structure comprises electroplated copper.

104. (currently amended) The electronic component ~~semiconductor chip or wafer~~ of claim 94, wherein said interconnecting metallization structure comprises aluminum.

105. (currently amended) The electronic component ~~semiconductor chip or wafer~~ of claim 94, wherein said metal layer is electroplated. ~~upper metallization structure comprises an electroplated metal.~~

106. (currently amended) An electronic component ~~semiconductor chip or wafer~~ comprising:

a semiconductor substrate having multiple semiconductor devices;

an interconnecting metallization structure over said semiconductor substrate and comprising a first contact pad;

an insulating ~~passivation~~ layer over said interconnecting metallization structure,

wherein said first contact pad is exposed by an opening in said insulating ~~passivation~~ layer; and

an upper metallization structure over said insulating ~~passivation~~ layer and comprising a gold layer with a thickness of between 2 and 100 μm, wherein said upper metallization structure comprises a second contact pad connected to said first contact pad, and wherein the positions of said first and second contact pads from a top view are different.

107. (currently amended) The electronic component ~~semiconductor chip or wafer~~ of claim 106, wherein said insulating ~~passivation~~ layer comprises a topmost nitride layer of said semiconductor chip or wafer.

108. (currently amended) The electronic component ~~semiconductor chip or wafer~~ of claim 106, wherein said insulating ~~passivation~~ layer comprises a passivation layer. ~~a topmost oxide layer of said semiconductor chip or wafer.~~

109. (currently amended) The electronic component ~~semiconductor chip or wafer~~ of claim 106, wherein said insulating ~~passivation~~ layer comprises a topmost CVD-formed ~~insulation~~ layer~~, formed using a CVD process,~~ of said semiconductor chip or wafer.

110. (currently amended) The electronic component ~~semiconductor chip or wafer~~ of claim 106, wherein said upper metallization structure further comprises a metal layer under said gold layer, wherein said metal layer comprises titanium tungsten.

111. (currently amended) The electronic component ~~semiconductor chip or wafer~~ of claim 106, wherein said semiconductor substrate comprises silicon.

112. (previously added) The electronic component ~~semiconductor chip or wafer~~ of claim 106, wherein said second contact pad is used to be wirebonded thereto.

113. (currently amended) The electronic component ~~semiconductor chip or wafer~~ of claim 106 further comprising a wirebond connected to said second contact pad.

114. (currently amended) The electronic component ~~semiconductor chip or wafer~~ of claim 106 further comprising a metal bump ~~formed~~ on said second contact pad.

115. (currently amended) The electronic component ~~semiconductor chip or wafer~~ of claim 106 further comprising a solder bump on said second contact pad..

116. (currently amended) The electronic component ~~semiconductor chip or wafer~~ of claim 106 further comprising a topmost polymer layer over said insulating ~~passivation~~ layer, wherein said upper metallization structure comprises an upper metal layer over said topmost polymer layer.

117. (currently amended) The electronic component ~~semiconductor chip or wafer~~ of claim 106, wherein said interconnecting metallization structure comprises electroplated copper.

118. (currently amended) The electronic component ~~semiconductor chip or wafer~~ of claim 106, wherein said interconnecting metallization structure comprises aluminum.

119. (currently amended) The electronic component ~~semiconductor chip or wafer~~ of claim 106, wherein said gold layer is electroplated. ~~formed using a process comprising electroplating.~~

120. (currently amended) An electronic component ~~semiconductor chip or wafer~~ comprising:

a semiconductor substrate having multiple semiconductor devices;

an interconnecting metallization structure over said semiconductor substrate and comprising a contact point;

a passivation layer over said interconnecting metallization structure, wherein said contact point is exposed by an opening in said passivation layer; and

a contact pad connected to said contact point, ~~an upper metallization structure over said contact point,~~ wherein said ~~upper metallization structure comprises a~~ contact pad comprises ~~comprising~~ a gold layer with a thickness of between 2 and 100 μm and ~~connected to said contact point, and wherein said contact pad~~ is used to be wirebonded thereto. ~~or has a metal bump formed thereon.~~

121. (currently amended) The electronic component ~~semiconductor chip or wafer~~ of claim 120, wherein said contact point comprises aluminum.

122. (currently amended) The electronic component ~~semiconductor chip or wafer~~ of claim 120, wherein said contact point comprises electroplated copper.

123. (currently amended) The electronic component ~~semiconductor chip or wafer~~ of claim 120 further comprising a ~~topmost~~ polymer layer over said passivation layer, wherein said contact pad is over said polymer layer. ~~upper metallization structure comprises an upper metal layer over said topmost polymer layer.~~

124. (currently amended) The electronic component ~~semiconductor chip or wafer~~ of claim 120, wherein said interconnecting metallization structure comprises electroplated copper.

125. (currently amended) The electronic component ~~semiconductor chip or wafer~~ of claim 120, wherein said interconnecting metallization structure comprises aluminum.

126. (currently amended) The electronic component ~~semiconductor chip or wafer~~ of claim 120, wherein said insulating ~~passivation~~ layer comprises a topmost nitride layer of said semiconductor chip or wafer.

127. (currently amended) The electronic component ~~semiconductor chip or wafer~~ of claim 120, wherein said insulating ~~passivation~~ layer comprises a topmost oxide layer of said semiconductor chip or wafer.

128. (currently amended) The electronic component ~~semiconductor chip or wafer~~ of claim 120, wherein said passivation layer comprises a topmost CVD-formed ~~insulation~~ layer~~,~~ ~~formed using a CVD process,~~ of said semiconductor chip or wafer.

129. (currently amended) The electronic component ~~semiconductor chip or wafer~~ of claim 120, wherein said gold layer is electroplated. ~~formed using a process comprising electroplating.~~

130. (canceled)

131. (currently amended) The electronic component ~~semiconductor chip or wafer~~ of claim 120 further comprising a wirebond connected to said contact pad.

132. (new) An electronic component comprising:

a substrate; and

a contact pad over said substrate, wherein said contact pad comprises a gold layer with a thickness of between 2 and 100 μm and is used to be wirebonded thereto.

133. (new) The electronic component of claim 132 further comprising a polymer layer over said substrate, wherein said contact pad is over said polymer layer.

134. (new) The electronic component of claim 132, wherein said gold layer is electroplated.

135. (new) The electronic component of claim 132, wherein said substrate comprises silicon.